PSpice Libraries for CoolMOS Power Transistors

Models provided by Infineon are not warranted by Infineon as fully representing all the specifications and operating characteristics of the semiconductor product to which the model relates. The models describe the characteristics of typical devices. In all cases, the current data sheet information for a given device is the final design guideline and the only actual performance specification.

Although models can be a useful tool in evaluating device performance, they cannot model exact device performance under all conditions, nor are they intended to replace breadboarding for final verification. Infineon therefore does not assume any liability arising from their use.

Infineon reserves the right to change models without prior notice.

1 Installation

The downloaded CoolMOS modelling package consists of the following files relevant to the PSpice simulator:

- ***.lib files comprising the PSpice code
- ***.slb files providing symbols for the models required by the graphic user interface (GUI) 'Schematics'. (In order to be usable in evaluation versions of the PSpice/Schematics system, each symbol library does not contain more than twenty symbols.)
- ***.olb files comprising symbols for the graphical user interface 'Capture'

If 'Schematics' is used as GUI, the ***.lib files must be installed via the 'Analysis → Library and Include Files' menu. Permanent installation via 'Add Library*' is recommended. The ***.slb files need to be installed via the menu 'Options → Editor Configuration → Library Settings'.

The installation in 'Capture' is similar. The ***.lib files must be included via the 'PSpice → Edit (New) Simulation Profile → Libraries' menu. Using the 'Add as Global' button will provide the CoolMOS models permanently. The symbol libraries (***.olb files) need to be included via 'Place → Part → Add Library'.

2 Definition of Modelling Levels

Infineon provides up to four different types of models for MOSFET devices. Three of them are based on a physical temperature-dependent model of the MOSFET structure and the package (so-called 'Level 1' till 'Level 3'). The fourth is a more empirical model that is less accurate, but faster and suitable for other Spice variants or simulators that can import Spice-like models ('Level 0')

Whereas Level 1 models assume a constant device temperature for the entire circuit and during a transient simulation (the temperature is to be given in the Analysis Setup), Level 2 models enable the user to define different temperatures for individual parts in the circuit. These temperatures can be changed dynamically during transient computations by connecting a voltage source to the Tj (junction temperature) pin. The voltage is converted into degree Celsius. If the Tj pin is not connected, a default temperature of 27 °C is used for the computation.

In order to be able to compute the selfheating dynamically, the electrical model is coupled with a thermal model of the device in Level 3 models. To do this, the current power dissipation in the transistor is determined permanently, and a current proportional to this power is fed into the thermal equivalent network. The voltage at the Tj node then contains the information about the time-dependent junction temperature which in turn acts directly on the temperature-dependent electrical model.

Level 3 models have two external thermal nodes: First, there is Tj, where the user can monitor the junction temperature easily. Usually, this node should not be connected. However, when the computation should start with a device junction temperature different to the thermal equilibrium, connecting Tj with a small capacitor (typically 1pF) to ground and stating an initial value (parameter IC) for the initial potential difference (which is used as a measure for the initial temperature in °C) enables these types of simulations. The second thermal pin is Tcase (or, in die models, Tpad). This pin has to be connected. An external resistor-capacitor-network can be added between the Tcase pin and ground potential The right-hand side terminal of the thermal network has to be connected to a thermal source to define the ambient temperature. (Fig. 1). On the other hand, shorting these pins leads to a network where optimum heat transfer is modelled.

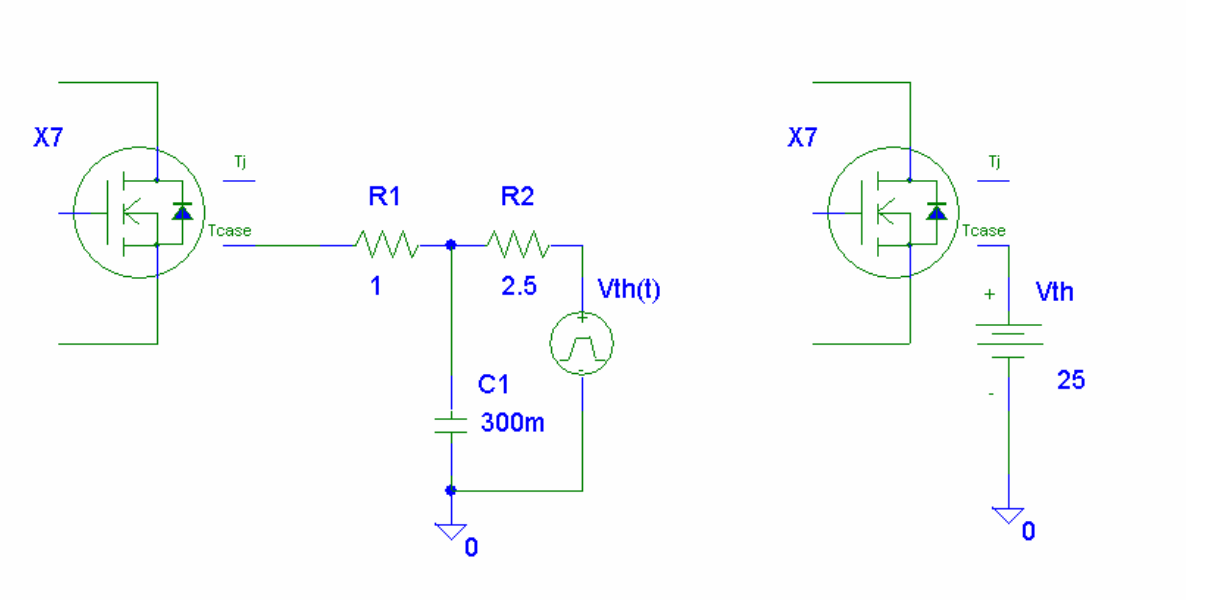

Fig. 1 Connecting external thermal networks

The part names of Level 3 models are similar to the device names. For example, the Level 3 model of the 600 V, 20 A CoolMOS SPP20N60S5 has the part name SPP20N60S5. Level 1 and Level 2 (if provided) models can be accessed using the suffixes L1 and L2, respectively. Hence, the models of the product above are named SPP20N60S5_L1 and SPP20N60S5_L2. For more details on the naming convention see the section 'Type Numbering System' given in the data book.

If the simulation focus is more on speed and not on accuracy, also simplified models are provided. These models can also be used in other Spice-like simulators that do not work

with PSpice specific sytax like function statements. The model name of the BSS87 is BSS87_L0, ie the suffix _L0 is used.

3 Optional Parameters for CoolMOS Models

CoolMOS model parameters are chosen to give the behaviour of a typical device. However, in order to enable worst-case analyses, CoolMOS models provide important parameters to the user.

Generally, the deviations are scaled to the range [-1;1] where a value of –1 refers to the minimum value, 0 is the typical value (default) and 1 accounts for the maximum value of the model parameter. Note that the parameters have different priorities, such that not all combinations are possible.

First, in Level 3 models the user can choose between the typical (physically minimum) transient thermal impedance and the maximum value guaranteed by Infineon. This can be done by changing the optional parameter `dZth` from its default value of 0 (typical Zth) to 1 (maximum Zth). Intermediate values are possible. User who prefer netlist input, can use this feature by adding `PARAMS: Zthtype=1` to the netlist line. In this example, the 1 would refer to the maximum Zth behaviour.

Second, the on-resistance of the device can be chosen between typical and maximum value. The allowed range for `dRdson` is [0;1] where, similarly to the `dZth` attribute, 0 is the typical and 1 the maximum value (netlist code: `PARAMS: dRdson=1).`

Thirdly, all types of models have the attribute `dVth` to model threshold voltage deviations from the typical value. Hence, a default value of 0 gives the typical device, -1 the minimum and 1 the maximum threshold voltage (netlist code: `PARAMS: dVth=1).` Setting a value `dRdson`≠0 overwrites `dVth`.

The modelling of device performance deviations is a complex task since typically there is no one-to-one relation between a deviation in the manufacturing process and the variation in a particular device parameter. The use of the given optional parameters does therefore not account for all cases and might in special cases even result in performance that does not fulfil the specifications guaranteed by Infineon.

4 Typical Simulation Parameters

As PSpice was originally not designed for power electronics and highly non-linear components, the standard simulation parameters (Simulation Setup/Options) are often not suitable. In common, the following typical values facilitate convergence:

ABSTOL=	1nA	(maximum current accuracy)
CHGTOL=	1pC	(maximum charge accuracy)
ITL1=	150	(maximum number of iterations for DC analyses without initial conditions)
ITL2=	150	(maximum number of iterations for DC analyses with initial conditions)
ITL4=	500	(maximum number of iterations for transient analyses time

		steps)
RELTOL=	0.01	(relative accuracy of voltages and currents)

In many cases it is necessary to limit the step size for transient analyses. The circuit system contains many different time scales, where the automatic step control of the PSpice simulator sometimes disregards essential fast-time-scale information which eventually leads to convergence problems. Typically, a step ceiling of the size of 1 ns is a remedy to this problem.

In cases where the time to be simulated (TSTOP) is relatively large (typically if thermal phenomena are of main interest) and sharp gradients are occurring, the minimum step size might be too large. In that cases it is helpful to start with a reduced TSTOP, interrupt the simulation process and change TSTOP to the desired value.

5 Modelling Contact Address

If you have further questions, feel free to contact us via our local sales offices, the internet (http://www.infineon.com/simulate) or email to simulate@infineon.com.